FPGA – System Designer

5-days session

Title	FPGA - System Designer
Overview	This training will allow current students, engineers and firmware designers to have the required skills and know-how for designing and coding HDL modules for complex FPGA architectures. We will cover also FPGA design examples for Deep Learning and Artificial Intelligence (AI). <u>The course/training will mainly focus on the following items:</u> ▪ FPGA architecture and resources: Xilinx vs Intel/Altera ▪ Xilinx Vivado design methodology ▪ Xilinx Zynq Processor ▪ Xilinx HLS, SDSoC and SDAccel design methodologies ▪ Xilinx Unified Software Tools (Vitis) ▪ FPGA – SoC communication ▪ High speed communication protocols ▪ Synthesis and Implementation ▪ Metastability and MTBF issues ▪ Design constraints ▪ Tcl scripting ▪ FloorPlanning ▪ Partial Reconfiguration ▪ Timing Closure ▪ Fan-out ▪ Pipelining ▪ Designing and packaging IPs for FPGA ▪ FPGA inference design methodology for AI
Labs	▪ Reset and clocking best practices ▪ Clock generation and constraining ▪ Clock Domain Crossing best practices ▪ Designing and constraining a DDR transfer ▪ MicroBlaze SoC Processor Design into FPGA ▪ Communicating between MicroBlaze and HDL modules ▪ Embedding a TCP/IP software stack into FPGA ▪ Implementing a high-speed 10G optical link into FPGA ▪ Implementing a PCIe design to communicate the FPGA board and the PC ▪ Hardware acceleration using SDSoC and SDAccel ▪ Running Embedded Linux on the FPGA board ▪ Running an AI engine into the FPGA board
Audience	Firmware/FPGA or software engineers that intend to have a system level mastering of FPGAs to ease for them to take the lead for any future FPGA based project
Prerequisite	▪ VHDL or Verilog experience ▪ Basic knowledge of FPGA architecture
Seats	[min = 8, max = 16]
Duration	5 days – 40 hours (50% courses, 50% Labs)