FPGA – DSP Designer

5-days session

Title	FPGA - DSP Designer
Overview	This training will allow current students, engineers and DSP designers to have the required skills and know-how for designing and implementing, on FPGA, complex DSP algorithms that are mainly used in 4G/5G systems. The know-how and methodology acquired during the training will help easing the design of other DSP blocks. The course/training will mainly focus on the following items: - Fixed- and Floating-point representations for DSP - Using High-Level Synthesis tools for designing DSP blocks - Using MATLAB for designing complex DSP blocks - Designing Digital Filters techniques - Diving into Xilinx and Altera DSP blocks - Multi-rate Signal Processing techniques - FFT design for FPGA - CORDIC implementation - Interfacing FPGA with high-speed ADC - Interfacing FPGA with high-speed DAC - Beamforming techniques - Complex Modulation schemes implementation - Forward Error Correction (FEC) techniques - Digital Predistortion techniques - Crest Factor Reduction techniques
Labs	- Designing & Implementing a FIR filter - Designing & Implementing a CIC filter - Designing & Implementing a Half-Band Filter - Designing & Implementing a poly-phase filter - Implementing a Radix-2 FFT - Designing & Implementing a Digital Up Converter (DUC) - Designing & Implementing a Digital Down Converter (DDC) - Carrier timing and phase recovery implementation - LTE signal demodulation - Implementing a channel estimator - Implementing a FEC module
Audience	Firmware/FPGA and DSP engineers that intend to implement DSP blocks inside FPGAs
Prerequisite	- VHDL or Verilog experience - Basic knowledge of FPGA architecture - Basic knowledge of digital signal processing theory
Seats	[min = 8, max = 16]
Duration	5 days – 40 hours (50% courses, 50% Labs)